Cover Sheet and Revision Status				
版別 (Rev.)	DCC No.	生效日 (Eff. Date)	變更說明 (Change Description)	發行人 (Originator)
1.0	20170009	Jun. 08, 2017	New issue	Hank Lin
2.0	20200019	Dec. 29, 2020	Revise ICC (operating current) 45ns- 20mA, 55ns- 20mA, 70ns- 15mA	Hank Lin

High Speed Super Low Power SRAM

256k Word x 16 bit

CS16LV41965

GENERAL DESCRIPTION

The CS16LV41965 is a high performance, high speed, super low power CMOS Static Random Access Memory organized as 262,144 words by 16 bits and operates from a wide range of 4.5 to 5.5V supply voltage. Advanced CMOS technology and circuit techniques provide both high speed and low power features with a typical CMOS standby current of 2uA and maximum access time of 45/55/70ns in 5.0V operation. Easy memory expansion is provided by an active LOW chip enable (/CE) and active LOW output enable (/OE) and three-state output drivers.

The CS16LV41965 has an automatic power down feature, reducing the power consumption significantly when chip is deselected. The CS16LV41965 is available in JEDEC standard 44-pin TSOP 2 and 48 ball TFBGA package.

FEATURES

- Low operation voltage : 4.5 ~ 5.5V
- Ultra low power consumption :
  - operating current: 20mA (Max.) @t_{AA}=45ns
  - standby current : 2uA (Typ.)
- Fast access time: 45/55/70ns (Max.)
- Automatic power down when chip is deselected.
- Three state outputs and TTL compatible, fully static operation
- Data retention supply voltage as low as 1.5V.

Product Family

Product Family	Operating Temp	Vcc. Range (V)	Speed (ns)	Standby (Max.)	Package Type
CS16LV41965	0~70°C	4.5~5.5	45/55/70	8 uA (Vcc = 5.5V)	44 TSOP 2-400mil
	-40~85°C				48 TFBGA_6x8mm

PIN CONFIGURATIONS

```
A4   ┌1          44┐ A5
A3   ┌2          43┐ A6
A2   ┌3          42┐ A7
A1   ┌4          41┐ /OE
A0   ┌5          40┐ /UB
/CE  ┌6          39┐ /LB
DQ0  ┌7          38┐ DQ15
DQ1  ┌8          37┐ DQ14
DQ2  ┌9          36┐ DQ13
DQ3  ┌10         35┐ DQ12
VCC  ┌11         34┐ VSS
VSS  ┌12   44L    33┐ VCC
DQ4  ┌13  TSOP    32┐ DQ11
DQ5  ┌14  2-400   31┐ DQ10
DQ6  ┌15   mil    30┐ DQ9
DQ7  ┌16         29┐ DQ8
/WE  ┌17         28┐ NC
A17  ┌18         27┐ A8
A16  ┌19         26┐ A9
A15  ┌20         25┐ A10
A14  ┌21         24┐ A11
A13  ┌22         23┐ A12
```

	1	2	3	4	5	6
A	/LB	/OE	A0	A1	A2	NC
B	D8	/UB	A3	A4	/CE	D0
C	D9	D10	A5	A6	D1	D2
D	Vss	D11	A17	A7	D3	Vcc
E	Vcc	D12	NC	A16	D4	Vss
F	D14	D13	A14	A15	D5	D6
G	D15	NC	A12	A13	/WE	D7
H	NC	A8	A9	A10	A11	NC

48-ball CSP

FUNCTIONAL BLOCK DIAGRAM

PIN DESCRIPTIONS

Name	Type	Function
A0 – A17	Input	Address inputs for selecting one of the 262,144 x 16 bit words in the RAM
/CE	Input	/CE is active LOW. Chip enable must be active when data read from or write to the device. If chip enable is not active, the device is deselected and in a standby power mode. The DQ pins will be in high impedance state when the device is deselected.
/WE	Input	The Write enable input is active LOW. It controls read and write operations. With the chip selected, when /WE is HIGH and /OE is LOW, output data will be present on the DQ pins, when /WE is LOW, the data present on the DQ pins will be written into the selected memory location.
/OE	Input	The output enable input is active LOW. If the output enable is active while the chip is selected and the write enable is inactive, data will be present on the DQ pins and they will be enabled. The DQ pins will be in the high impedance state when /OE is inactive.
/LB and /UB	Input	Lower byte and upper byte data input/output control pins.
DQ0~DQ15	I/O	These 16 bi-directional ports are used to read data from or write data into the RAM.
V_{CC}	Power	Power Supply
Gnd	Power	Ground

TRUTH TABLE

MODE	/CE	/WE	/OE	/LB	/UB	DQ0~7	DQ8~15	V_{CC} Current
Standby	X	X	X	H	H	High Z	High Z	I_{CCSB}, I_{CCSB1}
Standby	H	X	X	X	X	High Z	High Z	I_{CCSB}, I_{CCSB1}
Output Disabled	L	H	H	X	X	High Z	High Z	I_{CC}
Read	L	H	L	L	L	D_{OUT}	D_{OUT}	I_{CC}
Read	L	H	L	H	L	High Z	D_{OUT}	I_{CC}
Read	L	H	L	L	H	D_{OUT}	High Z	I_{CC}
Write	L	L	X	L	L	D_{IN}	D_{IN}	I_{CC}
Write	L	L	X	H	L	X	D_{IN}	I_{CC}
Write	L	L	X	L	H	D_{IN}	X	I_{CC}

ABSOLUTE MAXIMUM RATINGS [(1)]

Symbol	Parameter	Rating	Unit
V_{TERM}	TerMin.al Voltage with Respect to GND	-0.5 to Vcc+0.5	V
T_{BIAS}	Temperature Under Bias	-40 to +125	^{O}C
T_{STG}	Storage Temperature	-60 to +150	^{O}C
P_{T}	Power Dissipation	1.0	W
I_{OUT}	DC Output Current	30	mA

1. *Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.*

DC ELECTRICAL CHARACTERISTICS (T_A = 0℃ to 70℃, V_{CC} = 5.0V)

Parameter Name	Parameter	Test Conduction		MIN.	TYP [(1)]	MAX	Unit
V_{IL}	Guaranteed Input Low Voltage[(3)]			-0.3		0.8	V
V_{IH}	Guaranteed Input High Voltage[(2)]			2.2		Vcc+0.5	V
I_{IL}	Input Leakage Current	V_{CC}=MAX, V_{IN}=0 to V_{CC}		-1		1	uA
I_{OL}	Output Leakage Current	V_{CC}=MAX, /CE=V_{IN}, or /OE=V_{IN} , V_{IO}=0V to V_{CC}		-1		1	uA
V_{OL}	Output Low Voltage	V_{CC}=MAX, I_{OL} = 2mA				0.4	V
V_{OH}	Output High Voltage	V_{CC}=MIN., I_{OH} = -1mA		2.4			V
I_{CC}	Operating Power Supply Current	/CE=V_{IL}, I_{DQ}=0mA, F=F_{MAX}[(2)]	45ns			20	mA
			55ns			20	
			70ns			15	
I_{CCSB}	Standby Supply - TTL	/CE=V_{IH}, I_{DQ}=0mA,				0.3	mA

| I_{CCSB1} | Standby Current -CMOS | /CE≧V$_{CC}$-0.2V, V$_{IN}$≧V$_{CC}$-0.2V or V$_{IN}$≦0.2V | | 2 | 8 | uA |

1. *Typical characteristics are measured at Vcc=5V, T$_A$=25℃ and not 100% tested*

2. *Overshoot : VCC +2.0V in case of pulse width ≦20ns.*

3. *Undershoot : - 2.0V in case of pulse width ≦20ns.*

4. *Overshoot and undershoot are sampled, not 100% tested.*

OPERATING RANGE

| Range	Ambient Temperature	Vcc
Commercial	0~70ºC	4.5V ~ 5.5V
Industrial	-40~85ºC	4.5V ~ 5.5V

DATA RETENTION CHARACTERISTICS (T$_A$ = 0℃ to + 70℃)

Parameter Name	Parameter	Test Conduction	MIN.	TYP	MAX	Unit
V$_{DR}$	V$_{CC}$ for Data Retention	/CE≧V$_{CC}$-0.2V, V$_{IN}$≧V$_{CC}$-0.2V or V$_{IN}$≦0.2V	1.5			V
I$_{CCDR}$	Data Retention Current	/CE≧V$_{CC}$-0.2V, V$_{CC}$=1.5V V$_{IN}$≧ V$_{CC}$-0.2V or V$_{IN}$≦0.2V		2	6	uA
T$_{CDR}$	Chip Deselect to Data Retention Time	See Retention Waveform	0			ns
t$_R$	Operation Recovery Time		t$_{RC}$			ns

LOW V$_{CC}$ DATA RETENTION WAVEFORM (1) (/CE Controlled)
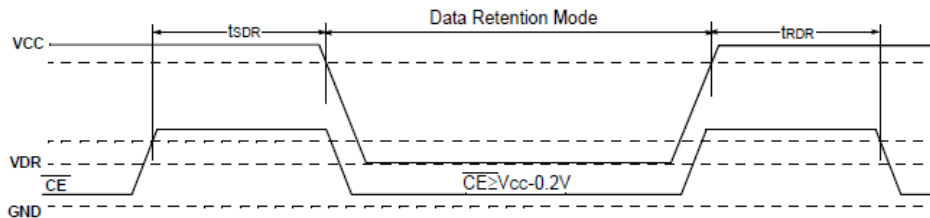
LOW V$_{CC}$ DATA RETENTION WAVEFORM (2) (/UB, /LB Controlled)
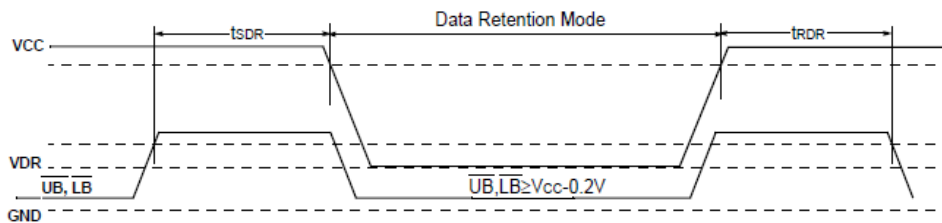
CAPACITANCE [1] (T$_A$ = 25°C, f =1.0 MHz)

Symbol	Parameter	Conditions	MAX.	Unit
C$_{IN}$	Input Capacitance	V$_{IN}$=0V	6	pF
C$_{DQ}$	Input/Output Capacitance	V$_{I/O}$=0V	8	pF

This parameter is guaranteed and not tested.

AC TEST CONDITIONS

Input Pulse Levels	Vcc/0V
Input Rise and Fall Times	3ns
Input and Output TiMin.g Reference Level	0.5Vcc
Output Load	See FIGURE 1A and 1B

KEY TO SWITCHING WAVEFORMS

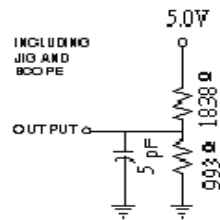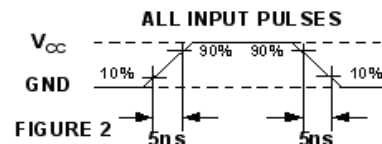| WAVEFORMS	INPUTS	OUTPUTS
	MUST BE STEADY	MUST BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGE FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGE FROM L TO H
	DON'T CARE ANY CHANGE PERMITTED	CHANGE STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE OFF STATE

AC TEST LOADS AND WAVEFORMS
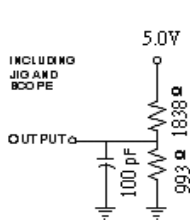
FIGURE 1A

FIGURE 1B

TERMINAL EQUIVALENT
OUTPUT ○──\/\/\/── 645 Ω ──○ 1.75V

ALL INPUT PULSES

Vcc　90%　90%

GND　10%　10%

FIGURE 2　5ns　5ns

7　　**Rev. 2.0**

AC ELECTRICAL CHARACTERISTICS ($T_A = 0°C$ to $+ 70°C$, $V_{CC} = 5.0V$)

< READ CYCLE >

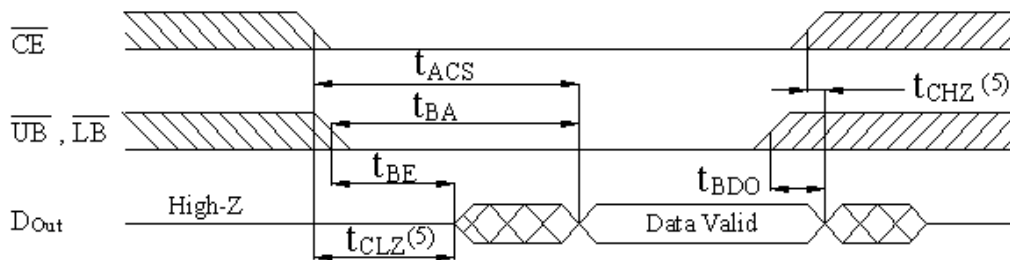| Parameter Name	Description	-45 MIN.	-45 MAX	-55 MIN.	-55 MAX	-70 MIN.	-70 MAX	Unit
t_{RC}	Read Cycle Time	45		55		70		ns
t_{AA}	Address Access Time		45		55		70	ns
t_{ACS}	Chip Select Access Time (/CE)		45		55		70	ns
t_{BA}	Data Byte Control Access Time (/LB, /UB)		45		55		70	ns
t_{OE}	Output Enable to Output Valid		22		25		35	ns
t_{CLZ}	Chip Select to Output Low Z (/CE)	10		10		10		ns
t_{BE}	Data Byte Control to Output Low Z (/LB, /UB)	5		5		5		ns
t_{OLZ}	Output Enable to Output in Low Z	5		5		5		ns
t_{CHZ}	Chip Deselect to Output in High Z (/CE)	0	18	0	20	0	25	ns
t_{BDO}	Data Byte Control to Output High Z (/LB, /UB)		18	0	20	0	25	ns
t_{OHZ}	Output Disable to Output in High Z		18	0	20	0	25	ns
t_{OH}	Out Disable to Address Change	10		10		10		ns

NOTES:

1.   /WE is high in read Cycle.

2.   Device is continuously selected when /CE = V_{IL}.

3.   Address valid prior to or coincident with CE transition low.

4.   /OE = V_{IL}.

5.   Transition is measured ±500mV from steady state with CL = 5pF as shown in Figure 1B. The parameter is guaranteed but not 100% tested.
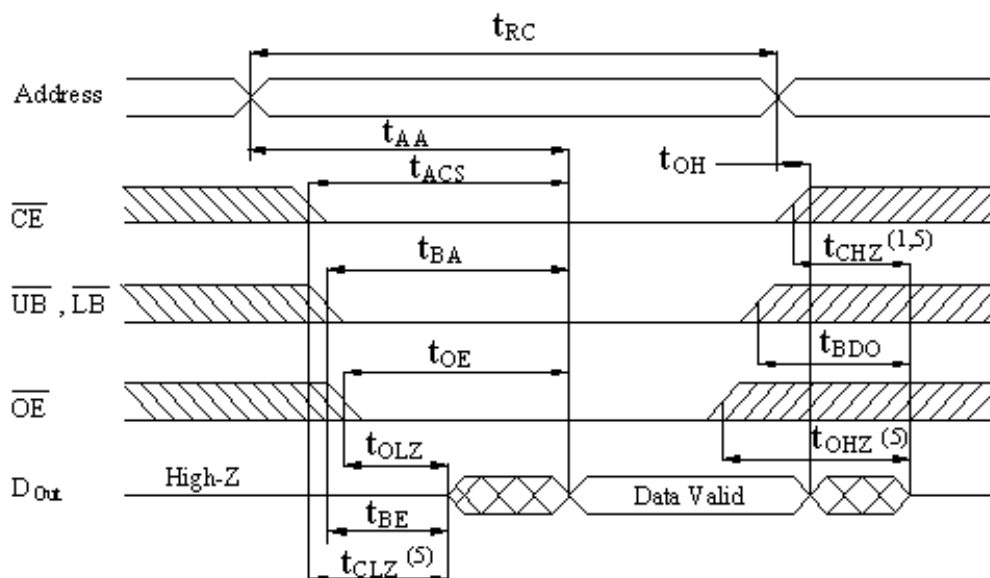
SWITCHING WAVEFORMS (READ CYCLE)

READ CYCLE 1. [1, 2, 4]

READ CYCLE 2. [1, 3, 4]

READ CYCLE 3. [1, 4]

AC ELECTRICAL CHARACTERISTICS $(T_A = 0 \ ℃to + 70℃, V_{CC} = 5.0V)$

< WRITE CYCLE >

Parameter Name	Description	-45 MIN.	-45 MAX	-55 MIN.	-55 MAX	-70 MIN.	-70 MAX	Unit
t_{WC}	Write Cycle Time	45		55		70		ns
t_{CW}	Chip Select to End of Write	35		45		60		ns
t_{AS}	Address Setup Time	0		0		0		ns
t_{AW}	Address Valid to End of Write	35		45		60		ns
t_{WP}	Write Pulse Width	35		40		50		ns
t_{WR1}	Write Recovery Time (/CE, /WE)	0		0		0		ns
t_{BW}	Data Byte Control to End of Write(/LB, /UB)	35		45		60		ns
t_{WHZ}	Write to Output in High Z		18		20		25	ns
t_{DW}	Data to Write Time Overlap	25		25		30		ns
t_{DH}	Data Hold from Write Time	0		0		0		ns
t_{OW}	End of Write to Output Active	5		5		5		ns

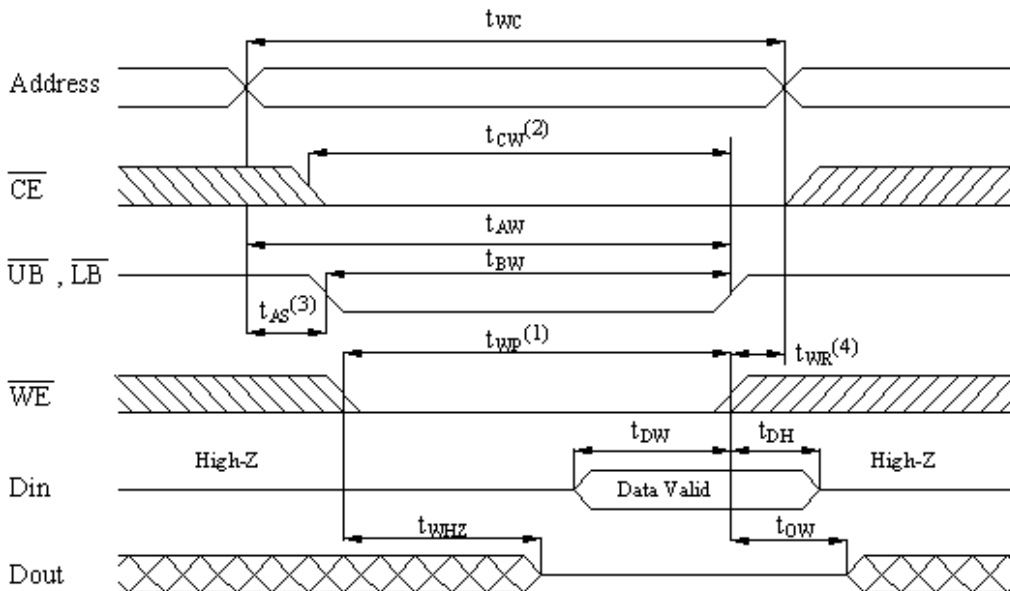■ **SWITCHING WAVEFORMS (WRITE CYCLE)**

WRITE CYCLE 1. (/WE Controlled)
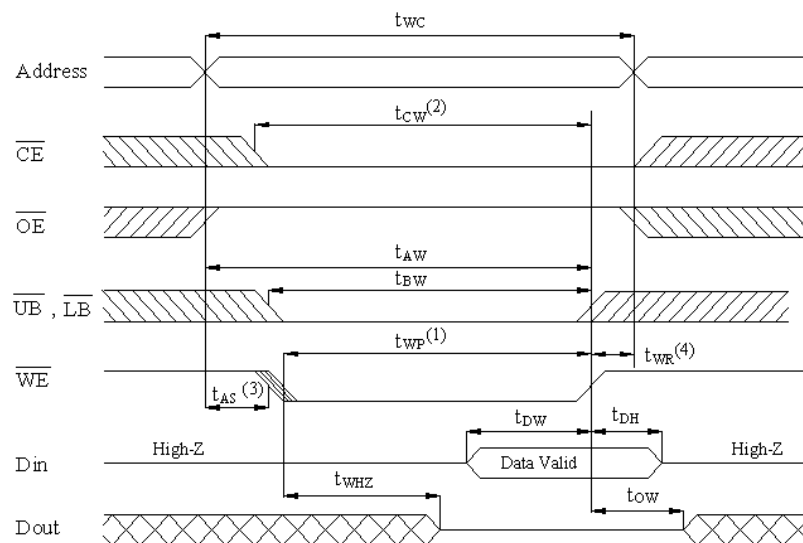
WRITE CYCLE 2. (/CE1 and CE2 Controlled)
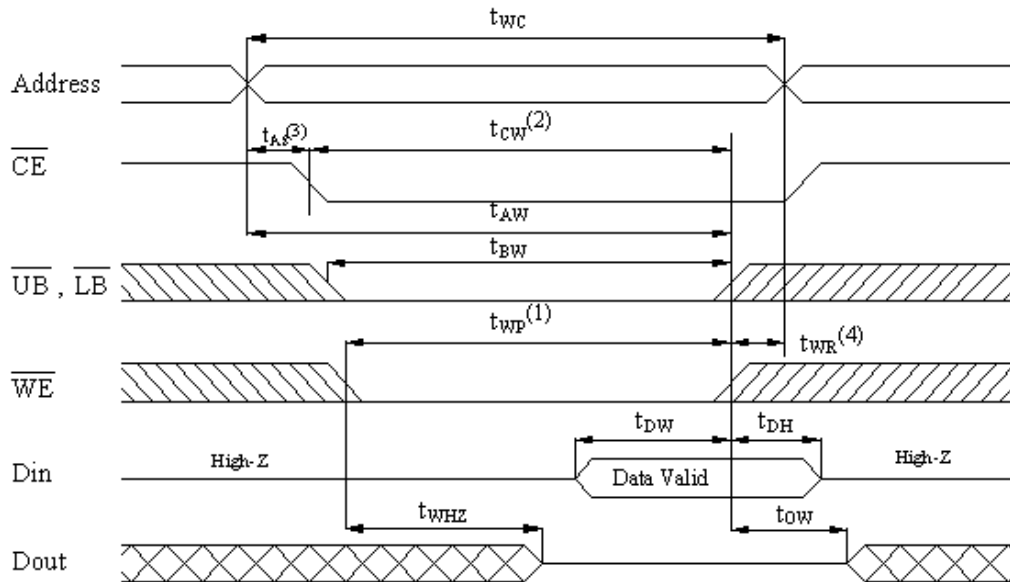
WRITE CYCLE 3. (/UB and /LB Controlled)

NOTES:

1. *T_{AS} is measured from the address valid to the beginning of write.*

2. *The internal write time of the memory is defined by the overlap of /CE and /WE low. All signals must be active to initiate a write and*
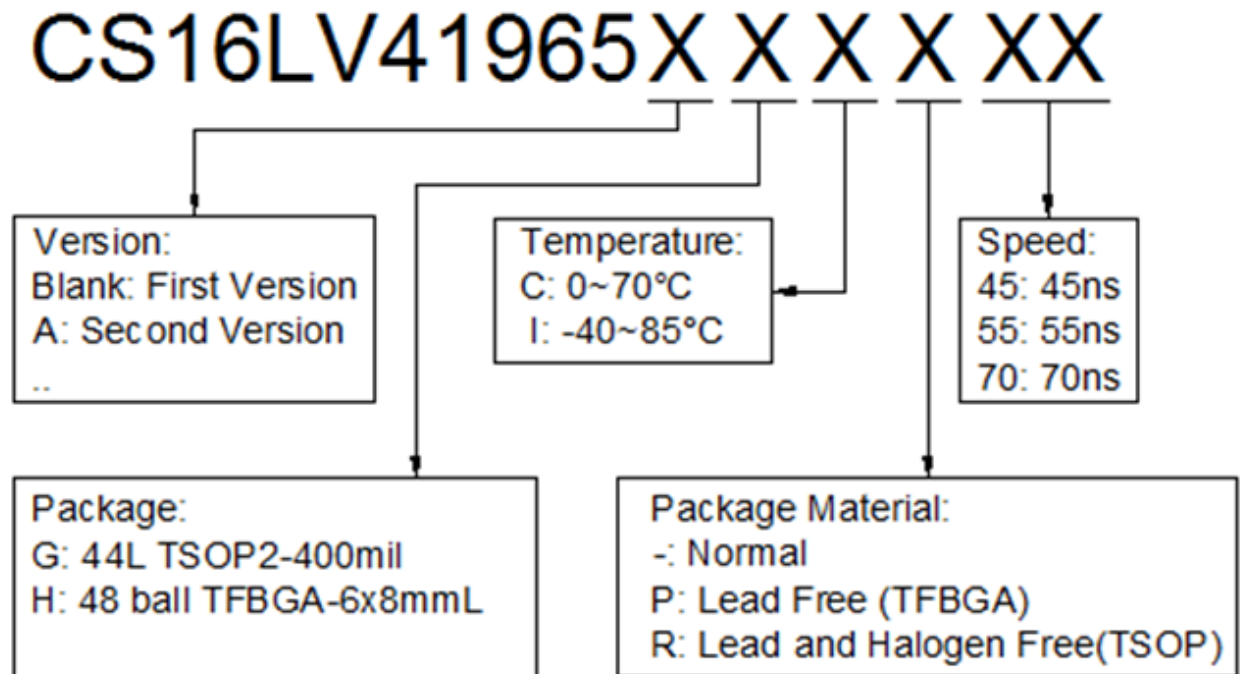
any one signal can terminate a write by going inactive. The data input setup and hold timing should be referenced to the second transition edge of the signal that terminates the write.

3. *TWR is measured from the earliest of /CE or /WE or (/UB and ,or /LB) going high at the end of write cycle.*

4. *During this period, DQ pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.*

5. *If the /CE low transition occurs simultaneously with the /WE low transitions or after the /WE transition, output remain in a high impedance state.*

6. */OE is continuously low (/OE = VIL).*

7. *DOUT is the same phase of write data of this write cycle.*

8. *DOUT is the read data of next address.*

9. *If /CE is low during this period, DQ pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.*

10. *Transition is measured ±500mV from steady state with CL = 5pF as shown in Figure 1B. The parameter is guaranteed but not 100% tested.*

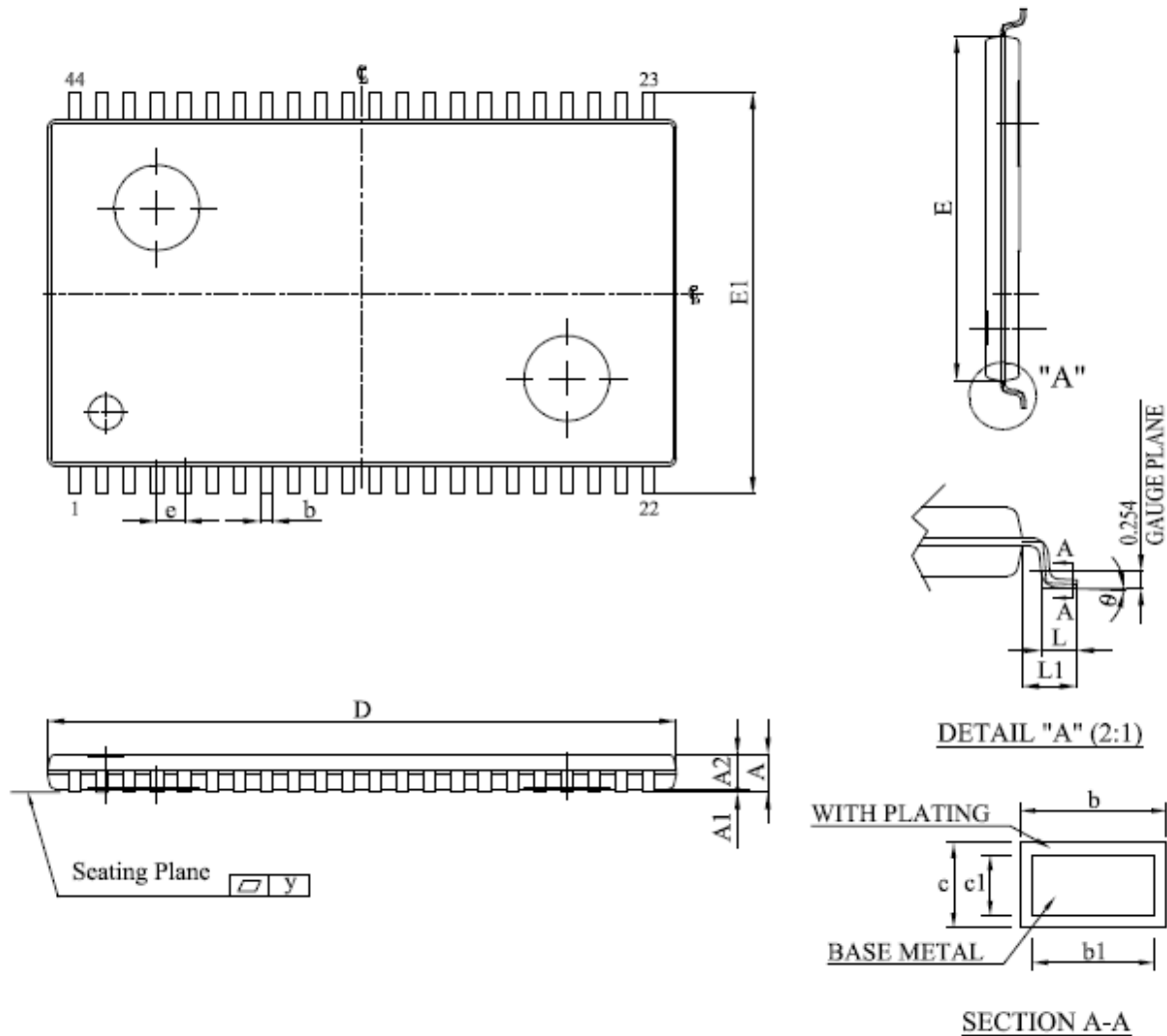11. *TCW is measured from the later of /CE going low to the end of write.*

ORDER INFORMATION

CS16LV41965X X X X XX

Version:
Blank: First Version
A: Second Version
..

Temperature:
C: 0~70°C
I: -40~85°C

Speed:
45: 45ns
55: 55ns
70: 70ns

Package:
G: 44L TSOP2-400mil
H: 48 ball TFBGA-6x8mmL

Package Material:
-: Normal
P: Lead Free (TFBGA)
R: Lead and Halogen Free(TSOP)

Note: Package material code "P" & "R" meets ROHS.

PACKAGE OUTLINE

44L TSOP2-400MIL

DETAIL "A" (2:1)

SECTION A-A

Note: Plating thickness spec : 0.3 mil ~ 0.8 mil.

SYMBOL UNIT		A	A1	A2	b	b1	c	c1	D	E	E1	e	L	L1	y	Θ
mm	Min.	1.00	0.05	0.95	0.30	0.30	0.12	0.12	18.31	10.06	11.56	0.70	0.40	0.70	–	0°
	Nom.	1.10	0.10	1.00	–	–	–	–	18.41	10.16	11.76	0.80	0.50	0.80	–	–
	Max.	1.20	0.15	1.05	0.45	0.40	0.21	0.16	18.51	10.26	11.96	0.90	0.60	0.90	0.1	8°
inch	Min.	0.0393	0.002	0.037	0.012	0.012	0.005	0.005	0.721	0.396	0.455	0.0275	0.0157	0.0275	–	0°
	Nom.	0.0433	0.004	0.039	–	–	–	–	0.725	0.400	0.463	0.0315	0.0197	0.0315	–	–
	Max.	0.0473	0.006	0.041	0.018	0.016	0.008	0.006	0.729	0.404	0.471	0.0355	0.0237	0.0355	0.004	8°

48 ball TFBGA-6x8mm

SIDE VIEW
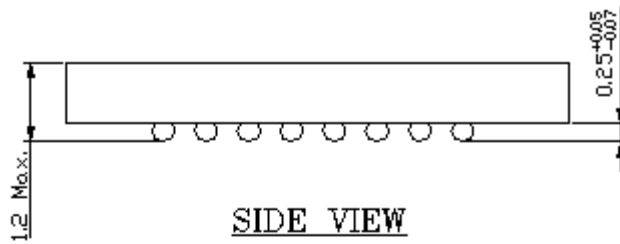
BALL PITCH		$e = 0.75$		
D	E	N	D1	E1
8.0	6.0	48	5.25	3.75

TOP VIEW

VIEW A
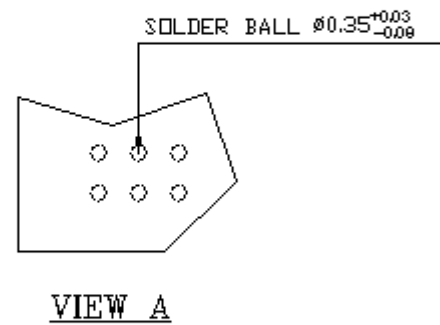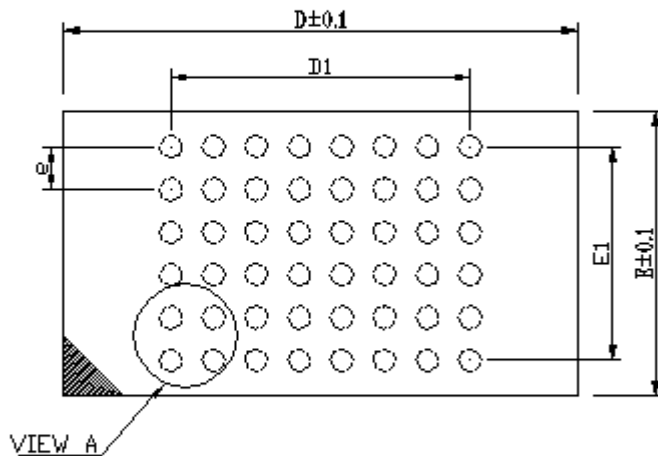
NOTES:
1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS.
2. PIN#1 DOT MARKING BY LASER OR PAD PRINT.
3. SYMBOL 'N' IS THE NUMBER OF SOLDER BALLS.